What is claimed is:

1. A method for modeling a physical memory for use in an electronic design, the method comprising the steps of:

modeling a memory write operation using a lookup table; and

modeling a memory read operation using the lookup table.

2. The method of claim 1, wherein the step of modeling a memory write operation comprises the steps of:

receiving a plurality of write address bits corresponding to a write address of the physical memory to which a plurality of write data bits are written by the electronic design;

receiving the plurality of write data bits corresponding to write data written to the physical memory at the write address; and

determining whether the lookup table comprises a first entry that contains the plurality of write address bits in an address field and a valid bit of the first entry is asserted.

3. The method of claim 2, wherein the step of modeling a memory write operation further comprises the step of:

writing the plurality of write data bits to a data field of the first entry if the first entry contains the plurality of write address bits in the address field and a valid bit of the first entry is asserted.

4. The method of claim 2, wherein the step of modeling a memory write operation further comprises the following steps if the first entry does not contain the plurality of write address bits in the address field and a valid bit of the first entry is not asserted:

finding a second entry in the lookup table wherein a valid bit of the second entry is not asserted;

writing the plurality of write address bits to an address field of the second entry;

writing the plurality of write data bits to a data field of the second entry; and

asserting the valid bit of the second entry.

5. The method of claim 1, wherein the step of creating a memory read operation comprises the steps of:

receiving a plurality of read address bits corresponding to a read address of the physical memory from which a plurality of read data bits are read by the electronic design; and

determining whether the lookup table comprises a first entry that contains the plurality of read address bits in an address field and a valid bit of the first entry is asserted.

6. The method of claim 5, wherein the step of creating a memory read operation further comprises the step of:

returning the plurality of read data bits from a data field of the first entry if the first entry contains the plurality of read address bits in the address field and a valid bit of the first entry is asserted.

7. The method of claim 5, wherein the step of creating a memory read operation further comprises the following steps if the first entry does not contain the plurality of read address bits in the address field and a valid bit of the first entry is not asserted:

finding a second entry in the lookup table wherein a valid bit of the second entry is not asserted;

writing the plurality of read address bits to an address field of the second entry;

assigning a plurality of read data bits corresponding to an arbitrary data value to a data field of the second entry;

asserting the valid bit of the second entry; and

returning the arbitrary data value.

8. The method of claim 7, wherein the arbitrary data value represents an initial value of the plurality of read data bits after an initialization step.

9. The method of claim 1, wherein a number of entries in the lookup is limited by a total number of memory operations that can occur over a given number of clock cycles, the total number of memory operations being computed by the steps of:

computing a total number of memory operations that can be performed per clock cycle; and

multiplying the total number of memory operations that can be performed per clock cycle by the given number of clock cycles.

10. The method of claim 9, further comprising the steps of:

determining a number of memory read operations in a property; and

adding the number of memory read operations in a property to the total number of memory operations.

11. The method of claim 1, further comprising the step of:

initializing a plurality of bits in a data field of an entry of the lookup table to an initial value.

12. A method for modeling an uninterpreted combinational block of an electronic circuit design in a lookup table, the uninterpreted combinational block being represented by a combinational function having an argument, the method comprising the steps of:

initializing the lookup table;

receiving the argument;

determining whether the lookup table comprises a first entry that contains the argument in an address field of the first entry and a valid bit of the first entry is asserted; and

returning a data value in a data field of the first entry if the first entry contains the argument and the valid bit of the first entry is asserted, the data value being associated with the argument.

13. The method of claim 12, further comprising the steps of writing the argument to an address field of a second entry having an unasserted valid bit, assigning an arbitrary data value to a data field of the second entry wherein the arbitrary data value is prospectively associated with the argument, asserting the valid bit of the second entry, and returning the arbitrary data value if the lookup table does not comprise a first entry that contains the argument in the address field of the first entry and the valid bit of the first entry is not asserted.

14. A method for modeling a physical memory in an electronic circuit design, the method comprising the steps of:

receiving a plurality of write address bits corresponding to a write address of the physical memory to which the electronic circuit design writes a plurality of write data bits;

receiving the plurality of write data bits written by the electronic circuit design to the physical memory at the write address;

modeling a memory write operation in a memory model to represent a memory write operation in the physical memory; and

determining whether the memory model comprises an entry that contains the plurality of write address bits in an address field and whether a valid bit of the entry is asserted.

15. The method of claim 14, wherein the plurality of write data bits are written to a data field of the entry if the entry contains the plurality of write address bits in the address field and the valid bit of the entry is asserted.

16. The method of claim 14, further comprising the following steps if the entry does not contain the plurality of write address bits in the address field and a valid bit of the entry is not asserted:

finding a second entry in the memory model wherein a valid bit of the second entry is not asserted;

writing the plurality of write address bits to an address field of the second entry;

writing the plurality of write data bits to a data field of the second entry; and

asserting the valid bit of the second entry.

17. The method of claim 14, further comprising the steps of:

receiving a plurality of read address bits corresponding to a read address of the physical memory from which the electronic circuit design reads a plurality of read data bits;

modeling a memory read operation in the memory model to represent a memory read operation in the physical memory; and

determining whether the entry contains the plurality of read address bits in the address field and whether the valid bit of the entry is asserted.

18. The method of claim 17, wherein the plurality of read data bits from a data field of the entry is returned if the entry contains the plurality of read address bits in the address field and the valid bit of the entry is asserted.

19. The method of claim 17, further comprising the following steps if the entry does not contain the plurality of read address bits in the address field and a valid bit of the entry is not asserted:

finding a second entry in the memory model wherein a valid bit of the second entry is not asserted;

writing the plurality of read address bits to an address field of the second entry;

assigning a plurality of read data bits corresponding to an arbitrary value to a data field of the second entry;

asserting the valid bit of the second entry; and

returning the arbitrary value.

20. The method of claim 14, wherein the memory model comprises a lookup table.

21. The method of claim 20, wherein a total number of entries of the lookup table is greater than or substantially equal to a total number of memory operations that can occur over a given number of clock cycles, the total number of memory operations being computed by the steps of:

determining a number of read ports of the physical memory;

determining a number of write ports of the physical memory;

computing a total number of memory operations that can be performed per clock cycle; and

multiplying the total number of memory operations that can be performed per clock cycle with the given number of clock cycles.

22. The method of claim 21, further comprising the steps of:

determining a number of memory read operations in a property; and

adding the number of memory read operations in a property to the total number of memory operations.

23. A method for modeling an electronic circuit design having a physical memory, the physical memory being represented by a lookup table, the method comprising the steps of:

creating the lookup table, the lookup table having a total number of entries that is greater than or substantially equal to an upper limit;

creating a hardware description language description of the memory model and a plurality of components of the electronic circuit design;

synthesizing a gate level description of the memory model and the plurality of components of the electronic circuit design;

verifying operation of the electronic circuit design using a set of properties.

24. The method of claim 23, wherein the step of creating the memory model comprises the steps of:

receiving a plurality of write address bits corresponding to a write address of the physical memory to which the electronic circuit design writes a plurality of write data bits;

receiving the plurality of write data bits written by the electronic circuit design to the physical memory at the write address;

receiving a plurality of read address bits corresponding to a read address of the physical memory from which the electronic circuit design reads a plurality of read data bits;

determining whether the lookup table comprises an entry that contains the plurality of read address bits in the address field and whether the valid bit of the entry is asserted;

returning the plurality of read data bits from a data field of the entry if the entry contains the plurality of read address bits in the address field and a valid bit of the entry is asserted;

determining whether the lookup table comprises an entry that contains the plurality of write address bits in an address field and whether a valid bit of the entry is asserted; and

writing the plurality of write data bits to the data field of the entry if the entry contains the plurality of write address bits in the address field and the valid bit of the entry is asserted.

25. The method of claim 24, further comprising the following steps if the entry does not contain the plurality of read address bits in the address field and a valid bit of the entry is not asserted:

finding a second entry in the lookup table wherein a valid bit of the second entry is not asserted;

writing the plurality of read address bits to an address field of the second entry;

assigning a plurality of read data bits corresponding to an arbitrary value to a data field of the second entry;

asserting the valid bit of the second entry; and

returning the arbitrary value.

26. The method of claim 24, further comprising the following steps if the entry does not contain the plurality of write address bits in the address field and a valid bit of the entry is not asserted:

finding a second entry in the memory model wherein a valid bit of the second entry is not asserted;

writing the plurality of write address bits to an address field of the second entry;

writing the plurality of write data bits to a data field of the second entry; and

asserting the valid bit of the second entry.

27. The method of claim 23, wherein the upper limit represents a total number of memory operations that can occur over a given number of clock cycles, the total number of memory operations being computed by the steps of:

determining a total number of memory read ports in the physical memory;

determining a total number of memory write ports in the physical memory;

computing a total number of memory operations that can be performed per clock cycle;

multiplying the total number of memory operations that can be performed per clock cycle with the given number of clock cycles.

28. The method of claim 27, further comprising the steps of:

determining a number of memory read operations performed in the set of properties; and

adding the number of memory read operations performed in the set of properties to the total number of memory operations.

29. A processor readable storage medium having processor readable code embodied on the processor readable storage medium, the processor readable code for programming a processor to perform a method for creating a memory model for use in modeling an electronic circuit design having a physical memory, the method comprising the steps of:

modeling a memory write operation using a lookup table; and

modeling a memory read operation using the lookup table.

30. The processor readable storage medium of claim 29, wherein the step of modeling a memory write operation comprises the steps of:

receiving a plurality of write address bits corresponding to a write address of the physical memory to which a plurality of write data bits are written by the electronic design;

receiving the plurality of write data bits written to the physical memory at the write address;

determining whether the lookup table comprises a first entry that contains the plurality of write address bits in an address field and a valid bit of the first entry is asserted; and

writing the plurality of write data bits to a data field of the first entry if the first entry contains the plurality of write address bits in the address field and the valid bit of the first entry is asserted.

31. The processor readable storage medium of claim 30, wherein the step of modeling a memory write operation further comprises the following steps if the first entry does not contain the plurality of write address bits in the address field and a valid bit of the first entry is not asserted:

finding a second entry in the lookup table wherein a valid bit of the second entry is not asserted;

writing the plurality of write address bits to an address field of the second entry;

writing the plurality of write data bits to a data field of the second entry; and

asserting the valid bit of the second entry.

32. The processor readable storage medium of claim 29, wherein the step of creating a memory read operation comprises the steps of:

receiving a plurality of read address bits corresponding to a read address of the physical memory from which a plurality of read data bits are read by the electronic design;

determining whether the lookup table comprises a first entry that contains the plurality of read address bits in an address field and a valid bit of the first entry is asserted; and

returning the plurality of read data bits from a data field of the first entry if the first entry contains the plurality of read address bits in the address field and the valid bit of the first entry is asserted.

33. The processor readable storage medium of claim 32, wherein the step of creating a memory read operation further comprises the following steps if the first entry does not contain the plurality of read address bits in the address field and the valid bit of the first entry is not asserted:

finding a second entry in the lookup table wherein a valid bit of the second entry is not asserted;

writing the plurality of read address bits to an address field of the second entry;

assigning a plurality of read data bits corresponding to an arbitrary value to a data field of the second entry;

asserting the valid bit of the second entry; and

returning the arbitrary value.

34. An apparatus for creating a memory model for use in modeling an electronic design having a physical memory, the apparatus comprising:

an output device;

a processor, in communication with the output device; and

a processor readable storage medium for storing code, the processor readable storage medium being in communication with the processor, the code capable of programming the processor to perform the steps of:

receiving a plurality of write address bits corresponding to a write address of the physical memory to which the electronic circuit design writes a plurality of write data bits;

receiving the plurality of write data bits written by the electronic circuit design to the physical memory at the write address;

receiving a plurality of read address bits corresponding to a read address of the physical memory from which the electronic circuit design reads a plurality of read data bits;

modeling a memory write operation using a memory model;

modeling a memory read operation using the memory model;

determining whether the memory model comprises an entry that contains the plurality of write address bits in an address field and whether a valid bit of the entry is asserted; and

determining whether the entry contains the plurality of read address bits in the address field and whether the valid bit of the entry is asserted.

35. The apparatus of claim 34, wherein the code capable of programming the processor performs the following steps if the entry does not contain the plurality of read address bits in the address field and a valid bit of the entry is not asserted:

finding a second entry in the memory model wherein a valid bit of the second entry is not asserted;

writing the plurality of read address bits to an address field of the second entry;

assigning a plurality of read data bits corresponding to an arbitrary value to a data field of the second entry;

asserting the valid bit of the second entry; and

returning the arbitrary value.

36. The apparatus of claim 34, wherein the code capable of programming the processor further comprises the step of:

returning the plurality of read data bits from a data field of the entry if the entry contains the plurality of read address bits in the address field and the valid bit of the entry is asserted.

37. The apparatus of claim 34, wherein the code capable of programming the processor performs the following steps if the entry does not contain the plurality of write address bits in the address field and a valid bit of the entry is not asserted:

finding a second entry in the memory model wherein a valid bit of the second entry is not asserted;

writing the plurality of write address bits to an address field of the second entry;

writing the plurality of write data bits to a data field of the second entry; and

asserting the valid bit of the second entry.

38. The apparatus of claim 34, wherein the code capable of programming the processor further comprises the step of:

writing the plurality of write data bits to a data field of the entry if the entry contains the plurality of write address bits in the address field and the valid bit of the entry is asserted.

39. The apparatus of claim 34, wherein the memory model comprises a lookup table.

40. The apparatus of claim 39, wherein a total number of entries of the lookup table is greater than or substantially equal to a total number of memory operations that can occur over a given number of clock cycles, the total number of memory operations being computed by the steps of:

determining a number of read ports of the physical memory;

determining a number of write ports of the physical memory;

computing a total number of memory operations that can be performed by the electronic design per clock cycle; and

multiplying the total number of memory operations that can be performed per clock cycle by the given number of clock cycles.

41. The apparatus of claim 40, further comprising the steps of:

determining a number of memory read operations in a property, the property being a set of behaviors of the physical memory; and

adding the number of memory read operations in a property to the total number of memory operations.

42. An apparatus for creating a model of an uninterpreted combinational block of an electronic circuit design using a lookup table, the uninterpreted combinational block being represented by a combinational function having an argument, the apparatus comprising:

an output device;

a processor, in communication with the output device; and

a processor readable storage medium for storing code, the processor readable storage medium being in communication with the processor, the code capable of programming the processor to perform the steps of:

receiving the argument;

determining whether the lookup table comprises a first entry that contains the argument in an address field of the first entry and a valid bit of the first entry is asserted; and

returning a data value in a data field of the first entry if the first entry contains the argument and the valid bit of the first entry is asserted, the data value being associated with the argument.

43. The apparatus of claim 42, wherein the code capable of programming the processor further comprises the step of:

initializing the lookup table.

44. The apparatus of claim 42, wherein the code capable of programming the processor further comprises the steps of writing the argument to an address field of a second entry having an unasserted valid bit, assigning an arbitrary data value to a data field of the second entry wherein the arbitrary data value is prospectively associated with the argument, asserting the valid bit of the second entry, and returning the arbitrary data value if the lookup table does not comprise a first entry that

contains the argument in the address field of the first entry and the valid bit of the first entry is not asserted.